

A STACKING STRUCTURE FOR SEMICONDUCTOR CHIPS AND A SEMICONDUCTOR PACKAGE USING IT

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Background of the Invention

1. Field of the Invention

The present invention relates to a semiconductor package and, more particularly, to a semiconductor package in which a plurality of semiconductor chips are stacked.

2. Description of the Related Art

As electronic devices get smaller, the components within these devices must get smaller as well. Because of this, there has been an increased demand for the miniaturization of components and greater packaging density. Integrated Circuit (IC) package density is primarily limited by the area available for die mounting and the height of the package. One way of increasing the density is to stack multiple die vertically in an IC package. Stacking multiple die will maximize function and efficiency of the semiconductor package.

Conventionally, a semiconductor package is constructed in such a manner that semiconductor chips sawed from a wafer are electrically connected with a substrate and, simultaneously, connected with a motherboard, being encapsulated up with an encapsulant. Recently, attempts have been made to stack a plurality of semiconductor chips serving as main components of the semiconductor package to maximize the performance of the semiconductor

package. A recent semiconductor package has multifunction and high performance owing to combination of a flash memory chip and a SRAM device, combination of a logic chip and a flash memory chip, combination of a digital chip and an analog chip or combination of a digital signal processor and a flash memory chip, for example. Furthermore, the semiconductor package having the semiconductor chips stacked therein is widely used for cellular phones, personal digital assistants, camcorders, PCs, routers and other portable products because it can satisfy a high memory density while having a small volume.

However, existing stack type semiconductor packages have the limitation of requiring an extraordinarily thick adhesive layer between the chips so as to prevent the conductive wire of the lower chip from contacting the bottom surface of the upper chip and thus creating an electrical short.

Therefore, a need existed to provide a device and method to overcome the above problem.

Summary of the Invention

A semiconductor package and method of producing the same has a substrate having a resin layer with first and second surfaces. A plurality of electrically conductive patterns are formed on the resin layer. An aperture is formed at the center of the substrate. A first semiconductor chip has first and second surfaces. The second surface of the first semiconductor chip has a plurality of input/output pads formed thereon. The first semiconductor chip is placed in the aperture of the substrate. A plurality of first conductive wires connect the input/output pads of the first semiconductor chip to the electrically conductive patterns formed on the second surface of the resin layer. A second semiconductor chip having first and second surfaces is coupled to the first semiconductor chip. The second

surface of the second semiconductor chip has a plurality of input/output pads formed thereon. A plurality of second conductive wires connect the input/output pads of the second semiconductor chip to the electrically conductive patterns formed on the second surface of the resin layer. An encapsulate is used to encapsulate the aperture of the substrate, the first and second semiconductor chips, and the first and second conductive wires. A plurality of conductive balls are coupled to the electrically conductive patterns formed on the second surface of the resin layer of the substrate.

The present invention is best understood by reference to the following detailed description when read in conjunction with the accompanying drawings.

Brief Description of the Drawings

FIG. 1A is an elevated perspective view of a semiconductor package according to an embodiment of the present invention;

FIG. 1B is an elevated bottom view of a semiconductor package according to an embodiment of the present invention;

FIG. 2A is a cross-sectional view taken along the line I-I of FIG. 1A;

FIG. 2B is an extended cross-sectional view of the portion II of FIG. 2A;

FIG. 2C is an extended cross-sectional view of a semiconductor package according to another embodiment of the present invention;

FIG. 3A is a cross-sectional view of a semiconductor package according to another embodiment of the present invention;

FIG. 3B is an extended cross-sectional view of the portion III of FIG. 3A;

FIG. 4A is a cross-sectional view of a semiconductor package according to another embodiment of the present invention;

FIG. 4B is an extended cross-sectional view of the portion IV of FIG. 4A;

FIG. 5 is a flow chart showing an example of one embodiment of a method of manufacture according to the present invention; and

FIGS. 6A to 6J are cross-sectional views corresponding to the flow chart of FIG. 5 showing one embodiment of the method of a manufacture of the present invention.

Common reference numerals are used throughout the drawings and detailed description to indicate like elements.

Detailed Description of the Invention

Referring to FIGS. 1A, 1B, 2A and 2B, a semiconductor package 101 according to an embodiment of the present invention is illustrated. As shown in the FIGS. 1A, 1B, 2A and 2B, the semiconductor package 101 has a substrate 20 with a planar plate shape, having an aperture 31 at the center thereof. The substrate 20 has a resin layer 23 including first and second surfaces 21 and 22. These first and second surfaces 21 and 22 of the resin layer 23 have a plurality of electrically conductive patterns 24 and 26 formed thereon. Electrically conductive patterns 24 and 26 of the first and second surfaces 21 and 22 are connected to each other through a conductive via 27. The aperture 31 is formed at the center of the resin layer 23 with its width being wider than that of a semiconductor chip that will be explained later.

The first and second surfaces 21 and 22 of the resin layer 23 and the electrically conductive patterns 24 and 26 are coated with a solder mask 30 to be protected from external environments. The solder mask 30 is not coated on a portion of the electrically conductive patterns 24 and 26 to which a conductive wire will be bonded or a conductive ball is fused. This will be explained later. Conventionally, the portion to which the conductive wire is bonded is called a bond finger 28 and the portion to which the conductive ball is fused is called a ball land 29. In addition, the solder mask 30 is not formed on a certain portion of the electrically conductive patterns 24 of the first surface 21 of the resin layer 23 so that a

conductive thin film 10 which will be described below can be connected to the electrically conductive pattern 24. This portion is defined as a land 25 in this description.

A conductive thin film 10 having the shape of a kind of plate is formed on one side of the substrate 20 to cover the aperture 31. In addition, the conductive thin film 10 is electrically connected to the electrically conductive patterns 24 formed on the first surface 21 of the resin layer 23. That is, the conductive thin film 10 is connected with the electrically conductive patterns 24 through the land 25 on which the solder mask 30 is not being coated. This conductive thin film 10 can be conventionally formed of Cu, Al, Ag, Ag-filled epoxy or its equivalent but the material is not limited thereto.

A first semiconductor chip 1 having a width smaller than that of the aperture 31 is located in the aperture 31 of the substrate 20. In other words, the first semiconductor chip 1 is placed on the surface of the conductive thin film 10 covering one side of the aperture 31. The first semiconductor chip 1 has first and second surfaces, 1a and 1b which are approximately planar. A plurality of input/output pads 1c are formed on the second surface 1b and a conductive ball 42 is fused to each of the input/output pads 1c. The conductive ball 42 is conventionally formed of gold, solder or its equivalent, but the material is not limited thereto.

Each of the electrically conductive patterns 26 formed on the second surface 22 of the resin layer 23 of the substrate 20 is connected with the conductive ball 42 formed on each input/output pad of the first semiconductor chip 1 through a first conductive wire 40. Specifically, one end of the first conductive wire 40 is ball-bonded 41 to the bond finger 28 of the electrically conductive pattern 26 and the other end is stitch-bonded 43 to the conductive ball 42. This wire bonding is generally called stand off stitch bonding (SSB).

The aforementioned SSB has an advantage of minimizing the height of the maximum curved portion of the first conductive wire formed at the second surface 1b of the first semiconductor chip 1. That is, the maximum curved portion of the first conductive wire is not

placed at the first semiconductor chip 1 but at the substrate 20. In other words, the maximum curved portion of the first conductive wire 40 is not located on the second surface 1b of the first semiconductor chip 1 but on the surface of the bond finger 28 of the electrically conductive pattern 26. Here, the first conductive wire may be formed of Au, Al, Cu or its equivalent but the material is not limited thereto.

An adhesive layer 4 with a predetermined thickness is attached onto the second surface 1b of the first semiconductor chip 1. The adhesive layer 4 can be a tape, epoxy or its equivalent, but the material is not limited thereto. The tape is generally used as the adhesive layers 4.

Referring to FIG. 2C, an extended cross-sectional view of a semiconductor package according to another embodiment of the present invention is illustrated.

As shown in the FIG.2C, instead of the adhesive layer 4, silicon 5 can come into contact with the second surface 1b of the first semiconductor chip 1. Here, the adhesive layer 4 can be formed on a top and bottom surface of the silicon 4. A dummy wafer sawed to a predetermined size can be used as the silicon 5.

A second semiconductor chip 2 is attached onto the adhesive layer 4. The second semiconductor chip 2 has first and second surfaces 2a and 2b that are approximately planar, and a plurality of input/output pads 2c are formed on the edge of the second surface 2b. An insulating layer 8 is attached onto the first surface 2a of the second semiconductor chip 2. The insulating layer 8 has the same area as that of the first surface 2a of the second semiconductor chip 2. This insulating layer 8 uses an insulating adhesive film having a predetermined degree of elasticity so that the first conductive wire 40 is not damaged or short-circuited even if it comes into contact with the insulating layer 8.

Furthermore, the insulating layer 8 is coated or printed on the overall surface of one side of the wafer (the first surface 2a of the second semiconductor chip 2) in advance. Specifically, the insulating layer 8 is formed on one side of the wafer through coating or

printing, and then the wafer is sawed into a plurality of second semiconductor chips 2 so that the insulating layer 8 is provided together with the second semiconductor chip 2. The insulating layer 8 can also be independently formed on each second semiconductor chip.

The distance between the first and second semiconductor chips 1 and 2 is generally around 3-4 mil to a minimum so that a total thickness of the semiconductor package is much thinner. That is, the total thickness of the adhesive layer 4 and the insulating layer 8 can reduce by about 3-4 mil at a minimum by using SSB.

Meantime, the probability of contact of the first conductive wire 40 and the first surface 2a of the second semiconductor chip 2 (specifically, the insulating layer 8) is decreased remarkably, compared to the conventional case. That is, the maximum curved portion of the first conductive wire 40 is not placed at the first semiconductor chip side but at the substrate side so that the probability of contact of the first conductive wire 40 and the insulating layer 8 is reduced. This advantage becomes powerful when the thickness of the substrate 20 is larger than that of the first semiconductor chip 1. This is because the maximum curved portion of the first conductive wire is formed at the first semiconductor chip side to increase the probability of contact of the first conductive wire 40, and the second semiconductor chip 2 if the first conductive wire 40 is boned using the conventional normal wire bonding even when the substrate 20 is thicker than the first semiconductor chip.

The electrically conductive pattern 26 of the substrate 20, specifically, the bond finger 28 of the electrically conductive pattern 26 formed on the second surface 22 of the resin layer 23 is connected to the input/output pad 2c of the second semiconductor chip 2 through a second conductive wire 50. One end of the second conductive wire 50 is ball-bonded 51 to the input/output pad 2c of the second semiconductor chip 2 and the other end is stitch-boned 52 to the bond finger 28 of the electrically conductive pattern 26 of the substrate 20. This type of wire bonding is called normal wire bonding. In this case, the maximum curved portion of the

second conductive wire 50 is located on the second surface 2b of the second semiconductor chip 2.

The aperture 31 of the substrate is filled with an encapsulant to construct an encapsulated portion 60 with a predetermined form. The encapsulant encapsulates up the first and second semiconductor chips 1 and 2, the first and second conductive wires 40 and 50 and the adhesive layer 4 to form the encapsulated portion 60 having the predetermined shape and, simultaneously, to protect them from external environments.

Finally, a conductive ball 70, such as solder ball, is fused to the electrically conductive pattern 26 of the substrate 20, specifically, the ball land 29 of the electrically conductive pattern 26 formed on the second surface 22 of the resin layer 23. The conductive ball 70 is fused to a mother board (not shown) in the subsequent process to transmit electric signals of the first and second semiconductor chips 1 and 2 to the mother board or deliver electric signals of the mother board to the first and second semiconductor chips 1 and 2. The conductive ball 70 is formed in a manner that its diameter is larger than the thickness of the part of the encapsulated portion 60 that is protruded downward so that the semiconductor package can be easily mounted on the mother board.

As described above, in the semiconductor package 101 of the present invention, the bond finger 28 of the electrically conductive pattern 26 of the substrate 20 is connected to the input/output pad 1c of the first semiconductor chip 1 through SSB to minimize the mutual interference or short-circuit between the first conductive wire 40 and the second semiconductor chip 2. That is, the maximum curved portion of the first conductive wire 40 is not formed on the second surface 1b of the first semiconductor chip 1 but on the electrically conductive pattern 26 of the substrate 20, to deteriorate the probability of contact of the first conductive wire 40 and the second semiconductor chip 2.

In addition, the conductive thin film 10 is naturally grounded on the motherboard according to the electrically conductive pattern 24, the conductive via 27, the electrically conductive pattern 26 and the conductive ball 70 to widely absorb external electromagnetic waves. That is, the conductive thin film 10 protects the first and second semiconductor chips 1 and 2 from external electromagnetic waves. Accordingly, electrical noise is removed when the first and second semiconductor chips 1 and 2 and the electrically conductive patterns 24 and 26 operate thereby improving the electrical performance of the semiconductor package 101. Furthermore, the first semiconductor chip 1 directly comes into contact with the wide conductive thin film 10 so that its heat radiating performance is also improved.

Referring to FIGS. 3A and 3B, a semiconductor package 102 according to another embodiment of the present invention is illustrated. The semiconductor package 102 is similar to the aforementioned semiconductor package 101 so that only the difference between them will be explained below.

As shown in the FIGS. 3A and 3B, the horizontal width of the second semiconductor chip 2 can be wider than that of the first semiconductor chip 1. Specifically, the second semiconductor chip 2 can be wider than the first semiconductor chip 1 in the horizontal direction by the width W. This is because the first conductive wire 40 connecting the bond finger 28 of the electrically conductive pattern 26 of the substrate 20 to the input/output pad 1c of the first semiconductor chip 1 is bonded through SSB. That is, the maximum curved portion of the first conductive wire 40 is not formed at the second surface 1b of the first semiconductor chip 1 but at the bond finger 28 of the electrically conductive pattern 26 of the substrate 20. If the normal wire bonding is carried out between the first semiconductor chip 1 and the substrate 20, it is impossible to use the second semiconductor chip 2 that is larger than the first semiconductor chip 1. This is because the first conductive wire 40 easily comes into contact with the first surface 2a of the second semiconductor chip 2 due to the maximum curved

portion of the first conductive wire 40 formed on the first semiconductor chip 1.

Referring to FIGS. 4A and 4B, a semiconductor package 103 according to another embodiment of the present invention is illustrated. The semiconductor package 103 is similar to the aforementioned semiconductor package 101 so that only the difference between them will be explained below.

As shown in the FIGS. 4A and 4B, one end of the second conductive wire 50 is ball-bonded 51 to the bond finger 28 of the electrically conductive pattern 26 of the substrate 20 and the other end is stitch-bonded 52 to the input/output pad 2c of the second semiconductor chip 2. Of course, a conductive ball 53 is formed on the input/output pad 2c of the second semiconductor chip 2 in advance so that the other end of the second conductive wire 50 can be stitch-bonded 52 to the conductive ball 53. In this embodiment, the thickness of the encapsulated portion 60 encapsulating up the second semiconductor chip 2 can be reduced more and the conductive ball 70 fused to the ball land 29 of the electrically conductive pattern 26 of the substrate 20 can have relatively small diameter. Accordingly, the semiconductor package 103 much thinner can be provided.

Referring to FIGS. 5 and 6A to 6J, one embodiment of a method for the manufacture of the present invention is illustrated. The semiconductor package is illustrated being turned upside down in FIGS. 6A to 6J differently from the one shown in FIGS. 1A to 4B, for convenience of explanation.

In the first step S1 of providing the substrate 20 having the aperture 31 formed at the center thereof, as shown in FIG. 6A, the substrate 20 including the resin layer 23 having the first and second surfaces 21 and 22 that are approximately planar is prepared. The fine electrically conductive patterns 24 and 26 are formed on the first and second surfaces 21 and 22 of the resin layer 23. The electrically conductive patterns 24 and 26 of the first and second surfaces 21 and 22 of the resin layer 23 of the substrate 20 are connected to each other through

the conductive via 27. In addition, the ball land 29, the bond finger 28 and the land 25 on which the insulating layer 30 is not coated are formed on the electrically conductive patterns 24 and 26. The aperture 31 with a predetermined area, in which a semiconductor chip that will be described below can be placed, penetrates the resin layer 23 at the center of the substrate 20.

5 In the second step S2, the aperture 31 of the substrate 20 is covered using an adhesive tape 90 having the shape of an approximately planar plate, as shown in FIG. 6B. This adhesive tape 90 attaches the first semiconductor chip 1 to the semiconductor package during a chip mounting process to stably support the first semiconductor chip 1. The adhesive tape 90 further prevents the encapsulant from flowing towards the bottom of the first semiconductor chip 1 during a encapsulating process.

10 In the third step S3, the first semiconductor chip 1 is placed in the aperture 31 of the substrate 20. The first semiconductor chip 1 having the first and second surfaces 1a and 1b is attached onto the surface of the adhesive tape 90 formed at the aperture 31 of the substrate 20, as shown in FIG. 6C. The first semiconductor chip 1 has a plurality of input/output pads 1c formed on the edge of the second surface 1b.

15 In the fourth step S4 for wire-bonding the bond finger 28 of the electrically conductive pattern 26 of the substrate 20 and the first semiconductor chip 1, one end of the first conductive wire 40 is ball-bonded 41 to the bond finger 28 of the electrically conductive pattern 26 of the substrate and the other end is stitch-bonded 43 to the input/output pads 1c of the first semiconductor chip 1. Specifically, the conductive ball 42 is formed on the input/output pads 1c of the first semiconductor chip 1. The conductive ball 42 is formed of gold, solder or its equivalent, but the material is not limited thereto. Then, one end of the first conductive wire 40 is ball-bonded 41 to the bond finger 28 of the electrically conductive pattern 26 of the substrate 20 and the other end is stitch-bonded 43 to the surface of the conductive ball 42 that was formed in advance. This wire bonding is carried out by using a capillary 80 of a wire bonder, as

shown in FIG. 6D. According to this first wire bonding step, the maximum curved portion of the first conductive wire 40 is not placed at the second surface 1b of the first semiconductor chip 1 but at the electrically conductive pattern 26 of the substrate 20.

In the fifth step S5 of forming the adhesive layer 4 on the second surface 1b of the first semiconductor chip 1, the adhesive layer 4 (for example, film, tape, elastomer, epoxy or its equivalent) is attached onto the second surface 1b of the first semiconductor chip 1, as shown in FIG. 6E. Instead of the adhesive layer 4, silicon (not shown) may come into contact with the second surface 1b of the first semiconductor chip 1. Here, the adhesive layer 4 can be formed on a top and bottom surface of the silicon.

In the sixth step S6 of attaching the second semiconductor chip 2 onto the adhesive layer 4, the second semiconductor chip 2 having the insulating layer 8 formed on the first surface 1a thereof is attached to the adhesive layer 4, as shown in FIG. 6F. Here, it is preferable that the second semiconductor chip 2 is obtained in a manner that the insulating layer 8 is formed on a wafer and then the wafer is sawed into the second semiconductor chip. It is also possible that the wafer is cut into individual semiconductor chips and then the insulating layer 8 is formed on each of the semiconductor chips.

In the step of attachment of the second semiconductor chip 2, the first surface 2a of the second semiconductor chip 2 (specifically, the insulating layer 8) does not come into contact with the first conductive wire 40. That is, the maximum curved portion of the first conductive wire 40 is not located at the first semiconductor chip 1 but at the substrate 20, to reduce the probability of contact of the first conductive wire 40 and the first semiconductor chip 1. Accordingly, it is possible to use the second semiconductor chip 2 having a horizontal width wider than that of the first semiconductor chip 1. Furthermore, even when the first conductive wire 40 comes into contact with the adhesive layer 8 of the second semiconductor chip 2, the first conductive wire 40 is prevented from being damaged or short-circuited if the insulating

layer 8 is formed of an insulating material with a certain degree of elasticity.

In the seventh step S7 of wire-bonding the input/output pads 2c of the second semiconductor chip 2 and the bond finger 28 of the electrically conductive pattern 26 of the substrate 20, one end of the second conductive wire 50 is ball-bonded 51 to the input/output pads 2c of the second semiconductor chip 2 and the other end is stitch-bonded 52 to the bond finger 28 of the electrically conductive pattern 26 of the substrate, as shown in FIG. 6G. Otherwise, a conductive ball (not shown) is formed on the input/output pads 2c of the second semiconductor chip 2 and then one end of the second conductive wire 50 is ball-bonded to the bond finger 28 of the electrically conductive pattern 26 and the other end is stitch-bonded to the conductive ball.

In the eighth step S8 of encapsulating up the first and second semiconductor chips 1 and 2 and the first and second conductive wires 40 and 50, the first and second semiconductor chips 1 and 2, the first and second conductive wires 40 and 50 and the adhesive layer 4 which are located in the aperture 31 of the substrate 20 are encapsulated up by using an encapsulant. As well known in the art, this encapsulating step is performed in a manner that the substrate 20 is placed in a mold (not shown) and then an epoxy molding compound with high-temperature and high-pressure is inserted into the mold, or liquid glop top is poured around the aperture 31 of the substrate 20 using a dispenser, to form the encapsulated portion 60 with a predetermined shape, as shown in FIG. 6H.

In the ninth step S9 of fusing the conductive ball 70 to the substrate 20, as shown in FIG. 6I, a flux is dotted on the exposed ball land 29 of the electrically conductive pattern 26 formed on the second surface 22 of the resin layer 23 of the substrate 20. Then, the conductive ball 70, such as solder ball, is put on the flux and introduced into a furnace with a high temperature so that the conductive ball 70 is fused to the ball land 29. Here, the flux temporarily fixes the conductive ball 70 and is volatilized in the furnace to be eliminated.

In the final step S10, as shown in FIG. 6J, the adhesive tape 90 is removed from the substrate 20 and the conductive thin film 10 is formed on the region from which the tape 90 was detached. The conductive thin film 10 can be formed by printing Ag-filled epoxy or attaching a plate-shaped thin film, for example, Cu, Al, Ag or its equivalent. Here, the
5 conductive thin film 10 is electrically connected to the electrically conductive pattern 24 of the substrate 20. That is, the conductive thin film 10 is connected to the electrically conductive pattern 24 through the land 25 exposed from the solder mask 30.

This disclosure provides exemplary embodiments of the present invention. The scope
10 of the present invention is not limited by these exemplary embodiments. Numerous variations, whether explicitly provided for by the specification or implied by the specification, such as variations in structure, dimension, type of material and manufacturing process may be implemented by one of skill in the art in view of this disclosure.